R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments and new claims may be found in the specification, for example, on page 5 lines 18-21, page 9 lines 2-10, page 10 lines 2-6, page 11 line 21 thru page 12 line 6, claims 1 and 5 and FIGS. 2 and 6 as originally filed. Thus, no new matter has been added.

OBJECTION TO THE SPECIFICATION

The objection to the specification for a non-descriptive title is respectfully traversed and should be withdrawn. Claim 1 provides a register stack and a control circuit for configuring the register stack. FIG. 1 illustrates the register stack and control circuit as part of a CPU. Therefore, the title of the application appears to be descriptive. The Examiner is respectfully requested to either (i) propose a new title, (ii) provide an explanation why the current title is allegedly non-descriptive or (iii) withdraw the objection.

OBJECTION TO THE DRAWINGS

The objection to the drawings is respectfully traversed and should be withdrawn. A PTO-948 form has not been provided with the Office Action to indicate what informalities should be corrected. Furthermore, the form paragraph 6.21 (see MPEP §608.02(b)) reproduced in the Office Action fails to identify what defect has been discovered in the content of the drawings. Therefore, the Examiner is respectfully requested to either (i) provide a PTO-948 form identifying the informalities, (ii) identify the detects discovered in the contents of the drawings or (iii) withdraw the objection.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-15 under 35 U.S.C. §102(b) as being anticipated by Vegesna et al. '142 (hereafter Vegesna) has been obviated by appropriate amendment and should be withdrawn.

The Federal Circuit has stated that "[t]o anticipate, ***every element and limitation*** of the claimed invention must be found in a single prior art reference, ***arranged as in the claim.***"[1] (Emphasis added). The Federal circuit has added that the

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[1] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant).

anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[2] Furthermore, "A claim is anticipated only if each and every element as set forth in the claim is found, either ***expressly or inherently*** described, in a single prior art reference."[3] (Emphasis added)

Vegesna concerns high performance register file with overlapping windows (Title). In contrast, claim 1 provides (in part) a control circuit configured to store a plurality of register states. However, Vegesna appears to be silent regarding storing register states. Therefore, Vegesna does not appear to disclose or suggest a control circuit configured to store a plurality of register states as presently claimed. Furthermore, the Office Action does not identify which element of Vegesna allegedly stores information similar to the claimed register states. The assertion on page 3, lines 5-6 of the Office Action, "therefore the system would have to be able to distinguish between the different states" does not appear to be an express or inherent argument as required by *Verdegaal Bros.* The Examiner is respectfully requested to

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[2] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[3] *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Circ. 1987).

either (i) identify which element in Vegesna expressly or inherently stores register states or (ii) withdraw the rejection.

Claim 1 further provides that the control circuit is configured to store a segment count signal. In contrast, Vegesna appears to be silent regarding storage of a signal similar to the claimed segment count signal. Therefore, Vegesna does not appear to disclose or suggest a control circuit configured to store a segment count signal as presently claimed. Furthermore, the assertion on page 3, lines 7-8 of the Office Action, "the pointer is incremented and decremented like a counter" fails to identify an element of Vegesna that stores a signal similar to the claimed segment count signal. Therefore, the Examiner is respectfully requested to either (i) identify which element in Vegesna expressly or inherently stores a segment count signal or (ii) withdraw the rejection.

Claim 1 further provides that the control circuit is configured to present a segment address signal. The Office Action asserts on page 3, lines 2-3 that the signals coming from a result vector driver 68 of Vegesna are similar to the claimed segment address signal. In contrast, column 10, lines 49-54 of Vegesna read:

> The Result Vector Driver 68 has a total of 1,024 output bit lines which are input into RAM Array 70. ***These lines comprise the data inputs*** for all of the memory locations which are addressable within the currently active register window. (Emphasis added)

Vegesna states that the signals coming from the result vector driver 68 are data, not addresses. One of ordinary skill in the art would distinguish data inputs from address inputs by virtue of the unique signal names. Therefore, the Examiner is respectfully requested to either (i) provide evidence why one of ordinary skill in the art would consider data input signals to be similar to address signals or (ii) withdraw the assertion that the signals coming from the result vector driver 68 are similar to the claimed segment address signal. Claim 15 provides language similar to claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 10 provides a step for comparing a register address with a plurality of register states to present a gating signal. In contrast, Vegesna appears to be silent regarding register states. Therefore, Vegesna does not appear to disclose or suggest a step for comparing a register address with a plurality of register states to present a gating signal as presently claimed. Furthermore, the assertion on page 6, lines 12-13 of the Office Action that the result vector driver 68 of Vegesna stores register states and compares the register states with a register address appears to be a conclusory statement lacking evidence. The Examiner is respectfully requested to either (i) identify where Vegesna expressly or inherently discloses the claimed steps for

storing and comparing as required by *Verdegaal Bros.* or (ii) withdraw the rejection.

Claim 10 further provides a step for gating a segment count with a gating count signal to present a segment address. In contrast, Vegesna appears to be silent regarding gating one signal with another signal. Therefore, Vegesna does not appear to disclose or suggest a step for gating a segment count with a gating count signal to present a segment address as presently claimed. Furthermore, the argument on page 6, lines 15-19 of the Office Action does not appear to identify a gating step. In particular, the argument identifies sources of various signals, but never actually cites any evidence in Vegesna of a gating operation. Therefore, the Examiner is respectfully requested to either (i) provide evidence where Vegesna expressly or inherently discloses a step for gating or (ii) withdraw the rejection. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 4 provides a register stack comprising (i) a first portion disposed within a processor and configured as at least one segment of a plurality of segments and (ii) a second portion disposed external to the processor and configured as at least one segment of the plurality of segments. In contrast, Vegesna appears to be silent regarding part of a memory array (asserted similar to the claimed register stack) located inside a processor and part

located outside the processor. Therefore, Vegesna does not appear to disclose or suggest a register stack comprising (i) a first portion disposed within a processor and configured as at least one segment of a plurality of segments and (ii) a second portion disposed external to the processor and configured as at least one segment of the plurality of segments as presently claimed. As such, claim 4 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 5 provides a status circuit configured to present a gating signal. In contrast, Vegesna appears to be silent regarding any circuit presenting a gating signal. Therefore, Vegesna does not appear to disclose or suggest a status circuit configured to present a gating signal as presently claimed. Furthermore, the argument on page 4, lines 1-13 of the Office Action appears to be silent regarding an element within the result vector driver 68 of Vegesna (asserted similar to the claimed control circuit) similar to the claimed status circuit. Therefore, the Examiner is respectfully requested to either (i) identify which element of Vegesna expressly or inherently presents a gating signal or (ii) withdraw the rejection.

Claim 16 (part of the original claim 5) provides a counter (within the control circuit) configured to present a segment count signal. In contrast, Vegesna appears to be silent regarding a counter. Therefore, Vegesna does not appear to

disclose or suggest a counter configured to present a segment count signal as presently claimed. Furthermore, the argument on page 4, lines 2-3 of the Office Action does not appear to show the claimed relationship between the counter and the control circuit. In particular, the result vector driver 68 of Vegesna is asserted to be similar to the claimed control signal and a signal CWP is asserted to be similar to the claimed segment count signal in the Office Action. However, nothing in Vegesna or the Office Action appears to explain how the signal CWP is presented from the result vector driver 68. Therefore, the Examiner is respectfully requested to either (i) explain where Vegesna discloses the signal CWP presented from the result vector driver 68 or (ii) withdraw the rejection.

Claim 6 provides a comparator configured to present a gating signal responsive to a plurality of register states and a register address signal. In contrast, Vegesna appears to be silent regarding a comparator, register states and a gating signal. Therefore, Vegesna does not appear to disclose or suggest a comparator configured to present a gating signal responsive to a plurality of register states and a register address signal as presently claimed. Claim 9 provides language similar to claim 6. Furthermore, the assertion on page 4, lines 17-22 of the Office Action that the result vector driver 68 of Vegesna stores register states and compares the register states with a register address

appears to be a conclusory statement lacking evidence. Therefore, the Examiner is respectfully requested to either (i) identify where Vegesna expressly or inherently discloses the claimed comparator, register states and gating signal or (ii) withdraw the rejections for both claims 6 and 9.

Claim 7 provides a memory device (within the status circuit within the control circuit) configured to store the register states and present the gating signal. In contrast, Vegesna appears to be silent regarding a memory element within the result vector driver 68. Therefore, Vegesna does not appear to disclose or suggest a memory device configured to store a plurality of register states and present a gating signal as presently claimed. Furthermore, the argument on page 5, lines 1-9 of the Office Action does not appear to address a memory device generating a gating signal. Therefore, the Examiner is respectfully requested to either (i) identify where Vegesna expressly or inherently discloses a memory element storing register states and presenting a gating signal or (ii) withdraw the rejection.

Claim 8 provides a plurality of logic gates (within the control circuit) configured to present a segment address signal as a predetermined address responsive to a gating signal having a global state. In contrast, Vegesna appears to be silent regarding the result vector driver 68 (asserted similar to the control circuit) (i) presenting address signals, (ii) presenting a gating

signal and (iii) presenting a segment address as a predetermined address. Therefore, Vegesna does not appear to disclose or suggest a plurality of logic gates configured to present a segment address signal as a predetermined address responsive to a gating signal having a global state as presently claimed. Furthermore, the argument on page 5, lines 12-18 of the Office Action fails to address a predetermined address for the asserted segment address. Therefore, the Examiner is respectfully requested to either (i) provide evidence of where Vegesna explicitly or inherently discloses how one of the signals generated by the result vector driver 68 (asserted similar to the claimed gating signal) causes signals 106, 108, 110 and 112 (asserted similar to the claimed segment address signal) to have a predetermined address or (ii) withdraw the rejection.

Claim 11 provides steps for (i) presenting a signal communicating a plurality of register states and (ii) selecting one of the register states as a gating signal. In contrast, Vegesna appears to be silent regarding both steps for (i) presenting register states in a signal and (ii) selecting one of the register states as a gating signal. Therefore, Vegesna does not appear to disclose or suggest steps for (i) presenting a signal communicating a plurality of register states and (ii) selecting one of the register states as a gating signal as presently claimed. Furthermore, the argument on page 7, line 5 of the Office Action

fails to cite Vegesna for an express or inherent step of presenting a signal communicating a plurality of register states. Therefore, the Examiner is respectfully requested to either (i) provide evidence where Vegesna expressly or inherently discloses the claimed steps or (ii) withdrawn the rejection.

Claim 12 provides a step for setting the register states in response to a reset handler operation. In contrast, Vegesna appears to be silent regarding both register states and a reset handler operation. Therefore, Vegesna does not appear to disclose or suggest a step for setting a plurality of register states in response to a reset handler operation as presently claimed. Furthermore, the argument on page 7, lines 13-18 of the Office Action appears to be silent regarding where Vegesna discloses a reset handler operation. Therefore, the Examiner is respectfully requested to either (i) provide evidence where Vegesna expressly or inherently discloses a reset handler operation or (ii) withdraw the rejection.

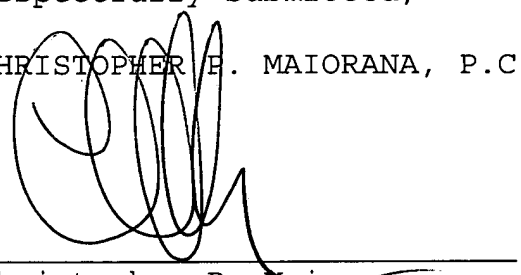
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Christopher P. Maiorana
Registration No. 42,829

Dated: June 18, 2004

c/o Pete Scott
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035

Docket No.: 99-339 / 1496.00059